

Synthesis of Ge/GeO_x Nanochain Kind of Structure for Fabrication of Single Electron Transistor

A.S.Katkar¹, B.N.Pawar²

1, 2 Department of Physics, Dr.B.N.Parandure Arts and Sci. S. G. G. Commerce and Science College, 410403, Maharashtra, India.
amarakatkar@gmail.com

Abstract

The Ge/GeO_x core-shell nanochain kind of structures were grown on P-type silicon (001) wafer by using a vapor transport method. The ultrasmall diameter of the Ge quantum dots connected with insulator germanium oxide (GeO_x) and its nanochain kind of structure has motivated to investigate possibilities to synthesize uniform Nanochain structure, so that it will be used to fabricate Ge nanochain SET device which holds one electron in each Ge QDs. These useful findings in the RT Ge/GeO_x nanochain SET devices may allow to envisage as in modern digital and analog circuits.

INTRODUCTION:

In a recent few years the size of conventional transistors has shrunk incredibly to nanometer scale, which makes modern electronics rapid, efficient and portable [1]. During 1980's the single electron tunneling and Coulomb blockade phenomena were major discoveries in modern physics [2,3]. As the SETs have advantages like ultra-low power consumption and high density integration, the SET device has been investigated extensively from last two decades [4]. Usually a simple SET device consist of a nanometer scale islands isolated by tunnel barriers with sufficiently large resistance ($R > h/e^2$). Until now varieties of SET devices working at RT has been demonstrated with different materials [5-10]. But its physical implementation is very difficult such as; to design and fabricate SET device with optimum junction capacitances and resistances with which thermal scattering effect on the tunnel junctions cannot be avoidable.

To develop the practical SET device it is significant to control the size of islands and tunnel junctions so that only single electron can confined within a small volume and localized on one side of the junction and can tunnel when an external applied voltage will be greater than e/C . The single-electron charging energy calculated within Si nanochain arise the hope that system like superlattice structure of quantum dots (Si core) with connecting insulating potential barriers (SiO₂) can used as a MTJ SET [11].

In this work, Ge/GeO_x core-shell nanochain kind of structures was grown on P-type silicon (001) wafer and also the possible mechanism for fabrication of Ge/GeO_x Nanochain was discussed.

EXPERIMENTAL:

The Ge/GeO_x core-shell nanochain kind of structures was grown by a vapor transport method using three zone furnace. A mixture of commercial Ge (99.999 %, Alfa Aesar) and C (99.999 %, Alfa Aesar) were used to synthesize Ge/GeO_x core-shell nanochain kind of structures with a 2:3 ratio. The

mixture was placed in an alumina boat, which was heated to a peak temperature of 1100 °C in zone-I. The 2 nm gold coated silicon wafers were placed at 550 °C in zone-II and zone-III. The samples were heated to 1100 °C at a rate of 20 °C/min with the reaction time of 60 min and with a 300 sccm (2.5 torr) Ar flowing through the tube.

RESULTS AND DISCUSSIONS:

Figure 1a depicts a low-magnification SEM image of the high density of Ge nanochains kind of morphology grown uniformly on the Si (001) substrate.

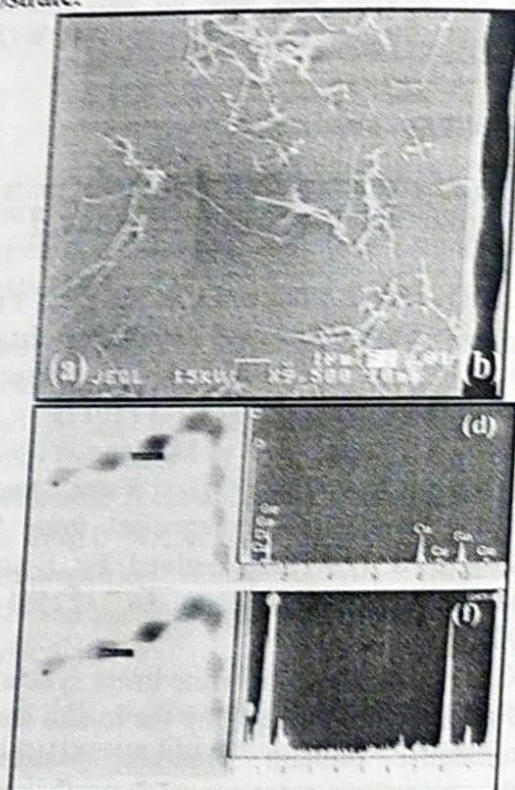


Figure:1 (a) SEM image of Ge nanochain kind of morphology (b) SEM image of Single Ge Nanochain (c&d) TEM image and EDS pattern of shell (neck) of Ge Nanochain (e&f) SEM image of Single Ge Nanochain TEM image and EDS pattern of core of Ge Nanochain

The length of the nanochains was measured to be in the range of 5-10 μm . The high-magnification SEM image (Figure 1b) depict nanochain morphology with bulbs and neck of diameters ranging from 15-20 nm and 5-8 nm respectively. The vapor

transport of mixture of solid sources ($\text{GeO}_2 + \text{C}$) under the appropriate and critical experimental conditions such as substrate temperature of 550°C , ambient pressure and the state of oxide of the outer layer of Ge nanowires resulted in the growth of high density of Ge nanochains kind of structure. Though the required growth of uniform Ge Nanochain structure could not be obtained, it increased the chances of it by optimizing the experimental conditions. In order to investigate the detailed structural and chemical data of the obtained structure, transmission electron microscopy (TEM) and energy dispersive X-ray spectroscopy (EDS) were used. Figure 1c & e depicts a TEM image of nanochain morphology which contains a number of bulb-like structures connected with thin narrow necks. The core of the bulb part having dark contrast is shown by dotted white lines. The EDS analysis (Figure 1 d&f) confirmed that, the core part is of Ge quantum dots and the outer shell of the Ge QDs and the narrow neck which connect Ge QDs consist of germanium oxide.

THE PROPOSED MECHANISM TO SYNTHESIS OF GE NANOCHAIN:

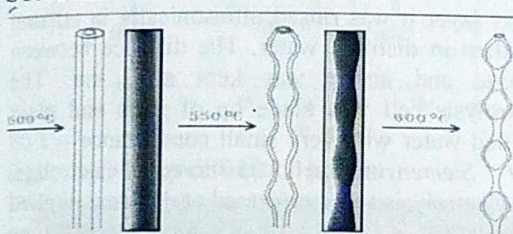


Figure 2. Schematic illustration of step by step growth of Ge nanowires to nanochains

At elevated temperature (500 to 600°C), a spheroidization process may occur to develop the Ge nanochains from nanowires. Surface and interface energy between Ge and GeO_x may play a vital role in the growth of Ge nanochains. As shown in Figure 1, at a substrate temperature of 500°C a Ge core with GeO_x shell was observed. As the substrate temperature increased, the perturbation along the nanowires was observed. So at higher temperatures of $600\text{--}700^\circ\text{C}$, during the spheroidization of the Ge core, Ge may diffuse towards the spheres and GeO_x may diffuse opposite to that of Ge to form a thin barrier between Ge nanospheres. There is a high possibility to grow the expected proper Ge nanochain by optimizing the experimental conditions. The morphology (size and shape) of the Ge nanochains (grown at a temperature of 550°C) raised the possibility of growth of proper Ge nanochains. Thus, the proposed mechanism is supporting the highest possibilities of synthesis of Germanium nanochain and fabrication of SET device. It would be very interesting to check the working of Ge nanochain device at room temperature.

CONCLUSIONS:

Thus, using a simple vapor transport method, the nanochain kind of structure was synthesized. In this project, the first priority was to optimize the experimental conditions to synthesize proper and nice nanochain structure, so that it can be used for further device fabrication. It was shown that there are a high amount of possibilities to synthesize uniform Ge Nanochains by optimizing experimental conditions. The investigation of electrical property of uniform Ge Nanochain device would be interesting in the future.

REFERENCES:

1. Feldheim, D. L.; Keating, C. D. Self-assembly of single electron transistors and related devices. *Chem. Soc. Rev.* **1998**, 27, 1.
2. Likharev, K. K. Single-Electron Transistors: Electrostatic Analogs of the DC SQUIDS. *IEEE Trans. Mag.* **1987**, 23, 1142.
3. Fulton, T. A.; Dolan, G. J. Observation of Single-Electron Effects in Small Tunnel Junctions. *Phys. Rev. Lett.* **1987**, 59, 109.
4. Yano, K.; Ishii, T.; Sano, T.; Mine, T.; Murai, F.; Hashimoto, T.; Kobayashi, T.; Kure, T.; Seki, K. Single-Electron Memory for Giga-to-Tera Bit Storage. *Proceed. IEEE* **1999**, 87, 633.
5. Guo, L.; Leobandung, E.; Chou, S. Y. A Silicon Single-Electron Transistor Memory Operating at Room Temperature. *Sci.* **1997**, 275, 649.
6. Postma, H. W. Ch.; Teepen, T.; Yao, Z.; Grifoni, M.; Dekker, C. Carbon Nanotube Single-Electron Transistors at Room Temperature. *Sci.* **2001**, 293, 76.
7. Graf, H.; Vancea, J.; Hoffmann, H. Single-electron tunneling at room temperature in cobalt nanoparticles. *Appl. Phys. Lett.* **2002**, 80, 1264.
8. Cui, J. B.; Burghard, M.; Kern, K. Room Temperature Single Electron Transistor by Local Chemical Modification of Carbon Nanotubes. *Nano Lett.* **2002**, 2, 117.
9. Tan, Y. T.; Kamiya, T.; Durrani, Z. A. K.; Ahmed, H. Room temperature nanocrystalline silicon single-electron transistors. *J. Appl. Phys.* **2003**, 94, 633.
10. Karre, P. S.; Bergstrom, P. L. Room temperature operational single electron transistor fabricated by focused ion beam deposition. *J. Appl. Phys.* **2007**, 102, 024316.
11. Sun, Z. Z.; Wang, X. R.; Zhang, R. Q.; Lee, S. T. Negative differential resistance and tunable peak-to-valley ratios in a silicon nanochain. *J. Appl. Phys.* **2008**, 103, 103719.